

R18

Code No: 156DF

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

B. Tech III Year II Semester Examinations, July - 2023

VLSI DESIGN

(Electronics and Communication Engineering)

Time: 3 Hours

Max. Marks: 75

Note: i) Question paper consists of Part A, Part B.

ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.

iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART - A

(25 Marks)

- 1.a) What is a pass transistor? [2]
- b) Mention the advantages of CMOS circuits. [3]
- c) Mention the importance of scaling. [2]
- d) Why metal - metal spacing is larger than ploy-ploy spacing? [3]
- e) Define Fan out. [2]
- f) Draw the circuits of any two logic gates. [3]
- g) Mention the applications of counters. [2]
- h) What are the limitations of DRAM? [3]
- i) Mention any two differences between FPGA and CPGA. [2]
- j) Mention the chip level test techniques in VLSI. [3]

PART - B

(50 Marks)

- 2.a) List and explain p-Well process fabrication steps.
- b) Determine the Pull-up to Pull-down ratio for an NMOS inverter driven through one or more pass transistors. [5+5]

OR

- 3.a) Draw a simple BiCMOS inverter circuit diagram and explain its operation.
- b) Discuss fabrication differences between NMOS and CMOS design technologies. [5+5]

- 4.a) Discuss the methodology to be followed in layout design.
- b) Explain about the scaling models and scaling factors. [5+5]

OR

- 5.a) Mention different choices of layers to be considered in wiring a circuit.
- b) Explain the importance of interconnects, wires and vias on the performance of a VLSI Circuit. [5+5]

- 6.a) Write a brief note on Inductive interconnect delay.
- b) Explain the effect of wiring capacitance on the performance of VLSI circuits. [5+5]

OR

- 7.a) Draw the circuit of a logic gate using pseudo NMOS logic and explain the operation.
- b) What are various switch logic circuits? Compare their merits and demerits. [5+5]

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- 8.a) Explain the design and operation of a Parity generator.
- b) Explain the design and operation of ROM.

[5+5]

QA QA QA QA QA QA QA QA QA G

- 9.a) Explain the design and operation of a Comparator.
- b) Explain the design and operation of a Serial Access Memory.

[5+5]

- 10.a) Explain the design approach of a PAL.
- b) What is testing? Explain the procedure to test combinational networks.

[5+5]

OR

QA QA QA QA QA QA QA QA QA G

- 11.a) Explain the design approach of a CPLD.
- b) Explain any one Chip level test technique.

[5+5]

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